UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,239	04/01/2004	Jeffery W. Janzen	MICS:0103 (02-1327)	9165

7590 03/20/2007

Michael G. Flether
Fletcher Yoder
P.O. Box 692289
Houston, TX 77269-2289

EXAMINER	
RAHMAN, FAHMIDA	
ART UNIT	**PAPER NUMBER**
2116	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/816,239	JANZEN ET AL.	
	Examiner	Art Unit	
	Fahmida Rahman	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to communications filed on 2/21/2007.

2. Claims 1-32 are pending.

Response to Amendment

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive as the arguments with respect to claims 6 and 12 are persuasive and, therefore, the finality of that action is withdrawn. Applicant's arguments with respect to claims 6 and 12 are moot in view of new grounds of rejections.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.
Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-32 of pending application are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-12 of U.S. Patent No.7035159). Although the conflicting claims are not identical, they are not patentably distinct from each other because both of the invention discloses a system with memory module comprising plurality of memory devices with non-volatile memory device that stores operating current values for the memory devices. For example, claim 25 of pending application recites the limitations "a memory module comprising plurality of volatile memory devices and a non-volatile memory device having operating current values uniquely corresponding to each of memory devices", which can be found in claims 1-5 of issued patent. For claims 26-28 of pending application, claims 4, 5 and 3 of the issued patent disclose the invention.

Claims 1-32 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-30 of copending Application No. 10816241. Although the conflicting claims are not identical, they are not patentably distinct from each other because both the applications recite a memory module comprising plurality of volatile memory devices and a non-volatile memory device having operating current values stored thereon corresponding to the plurality of volatile memory devices. For example, the limitations of claim 21 of pending application are present in claim 18 of the co-pending application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5, 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Trick (US Patent 5995405), in view of Abrahams et al (US Patent Application Publication 2004/0078454), further in view of Nerl (US Patent Application Publication 20020016897)

For claim 1, Trick teaches the following limitations:

A method of configuring a system comprising: reading values from a non-volatile memory device on a memory module (lines 35-42 of column 1), wherein the memory module comprises a plurality of volatile memory devices (lines 20-27 of column 1), and wherein the operating parameters uniquely corresponding to a lot in which the volatile memory devices were manufactured (EPROM is associated with the IMM. Thus, EPROM uniquely identifies the lot comprising plurality of volatile memory devices); and

configuring the system in accordance with the values from the non-volatile memory device on the memory module (lines 39-42 of column 1).

Trick does not teach the following limitations:

Reading operating current value from the non-volatile memory.

Abrahams et al disclose the following limitations:

A method of configuring a system comprising: reading operating current values from a non-volatile memory device on a memory module (lines 13-15 of [0009] of page 1 mention that the non-volatile memory stores input current) and configuring the system in accordance with the operating current values from the non-volatile memory device on the memory module ([0032] of page 3).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Trick and Abrahams et al. One ordinary skill in the art would be motivated to have the non-volatile memory comprising operating current corresponds to the components, since that would ensure if a component (i.e., volatile memory) is operating within prescribed range. The component of Abrahams et al that stores the operating currents is an FRU ([0009] of page 1). It is well known in the art that a DIMM can be an FRU (lines 12-13 of [0006] of page 1 of Nerl). Thus, the system of Abraham et al can have DIMM as a component, where the associated non-volatile memory of the component can store the operating currents.

For claim 2, EPROM of Trick is the serial presence detect device (lines 34-36 of column 1).

For claim 3, Trick teaches the dual inline memory module (lines 25-30 of column 1).

For claim 4, Trick teaches reading values during booting (lines 39-42 of column 1).

For claim 5, lines 12-19 of page 1 of Abrahams et al mention that the current operating condition is compared with specified operating condition and an error message is sent if the component is operating outside of the specified value. Thus, the specified values are the threshold values of the system.

For claim 21, Trick teaches the following limitations:
a memory module (lines 35-42 of column 1), wherein the memory module comprises a plurality of volatile memory devices (lines 20-27 of column 1), and wherein the operating parameters uniquely corresponding to a lot in which the plurality of the volatile memory devices were manufactured stored thereon (EPROM is associated with the IMM. Thus, EPROM uniquely identifies the lot comprising plurality of volatile memory devices);

Trick does not teach the following limitations:
Non-volatile memory device having operating current values

Abrahams et al disclose the following limitations:

A memory module comprising a non-volatile memory device having operating current values of the component (lines 13-15 of [0009] of page 1 mention that the non-volatile memory stores input current).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Trick and Abrahams et al. One ordinary skill in the art would be motivated to have the non-volatile memory comprising operating current corresponds to the component, since that would ensure if a component (i.e., volatile memory) is operating within prescribed range. The component of Abrahams et al that stores the operating currents in the non-volatile memory is an FRU ([0009] of page 1). It is well known in the art that a DIMM can be an FRU (lines 12-13 of [0006] of page 1 of Nerl). Thus, the system of Abraham et al can have DIMM as a component, where the associated non-volatile memory of the component can store the operating currents.

For claims 22-24, note lines 19-37 of column 1 of Trick.

4. Claims 7-11, 25-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Trick (US Patent 5995405), in view of Abrahams et al (US Patent Application Publication 2004/0078454)

For claim 7, Trick teaches the following limitations:

A method of configuring a system comprising: reading values from a non-volatile memory device on a memory module (lines 35-42 of column 1), wherein the memory module comprises a plurality of volatile memory devices (lines 20-27 of column 1), and wherein the operating parameters uniquely corresponding to each of the plurality of memory devices (EPROM is associated with the IMM. Thus, EPROM uniquely identifies each of the plurality of volatile memory devices); and configuring the system in accordance with the values from the non-volatile memory device on the memory module (lines 39-42 of column 1).

Trick does not teach the following limitations:

Reading operating current value from the non-volatile memory.

Abrahams et al disclose the following limitations:

A method of configuring a system comprising: reading operating current values from a non-volatile memory device on a memory module (lines 13-15 of [0009] of page 1 mention that the non-volatile memory stores input current), wherein the memory module (101) comprises a plurality of memory devices (100A-100I), and wherein the operating current parameters comprise operating currents uniquely corresponding each of the plurality of memory devices (150 uniquely corresponds to 100G); and configuring the system in accordance with the operating current values from the non-volatile memory device on the memory module ([0032] of page 3).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Trick and Abrahams et al. One ordinary skill in the art would be motivated to have the non-volatile memory comprising operating current corresponds to the components, since that would ensure if a component (i.e., volatile memory) is operating within prescribed range.

For claim 8, EPROM of Trick is the serial presence detect device (lines 34-36 of column 1).

For claim 9, Trick teaches the dual inline memory module (lines 25-30 of column 1).

For claim 10, Trick teaches reading values during booting (lines 39-42 of column 1).

For claim 11, lines 12-19 of page 1 of Abrahams et al mention that the current operating condition is compared with specified operating condition and an error message is sent if the component is operating outside of the specified value. Thus, the specified values are the threshold values of the system.

For claim 25, Trick teaches the following limitations:
a memory module (lines 35-42 of column 1), wherein the memory module comprises a plurality of volatile memory devices (lines 20-27 of column 1), and wherein the operating parameters uniquely corresponding to each of the plurality of the volatile memory

devices stored thereon (EPROM is associated with the IMM. Thus, EPROM uniquely identifies the plurality of volatile memory devices);

Trick does not teach the following limitations:

Non-volatile memory device having operating current values

Abrahams et al disclose the following limitations:

a non-volatile memory device on a memory module (lines 13-15 of [0009] of page 1 mention that the non-volatile memory stores input current), wherein the memory module (101) comprises a plurality of memory devices (100A-100I), and wherein the operating current parameters comprise operating currents uniquely corresponding to each of the memory device (150 uniquely corresponds to 100G);

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Trick and Abrahams et al. One ordinary skill in the art would be motivated to have the non-volatile memory comprising operating current corresponds to the components, since that would ensure if a component (i.e., volatile memory) is operating within prescribed range.

For claims 26-28, note lines 19-37 of column 1 of Trick.

For claim 29, Trick teaches the following limitations:

A computer system comprising: a processor (202 in Fig 4) and a memory module (lines 35-42 of column 1), wherein the memory module comprises a plurality of volatile memory devices (lines 20-27 of column 1), and wherein the operating parameters uniquely corresponding to each of the plurality of the volatile memory devices stored thereon (EPROM is associated with the IMM. Thus, EPROM uniquely identifies the lot comprising plurality of volatile memory devices);

Trick does not teach the following limitations:

Non-volatile memory device having operating current values

Abrahams et al disclose the following limitations:

a non-volatile memory device on a memory module (lines 13-15 of [0009] of page 1 mention that the non-volatile memory stores input current), wherein the memory module (101) comprises a plurality of memory devices (100A-100I), and wherein the operating current parameters comprise operating currents uniquely corresponding to each of the memory device (150 uniquely corresponds to 100G);

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Trick and Abrahams et al. One ordinary skill in the art would be motivated to have the non-volatile memory comprising operating current corresponds to the components, since that would ensure if a component (i.e., volatile memory) is operating within prescribed range.

For claims 30-32, note lines 19-37 of column 1 of Trick.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Trick (US Patent 5995405), in view of Abrahams et al (US Patent Application Publication 2004/0078454), in view of Nerl (US Patent Application Publication 20020016897), further in view of Wu (US Patent 7064994).

Neither Trick nor Abrahams et al teach the throttling of the memory. Wu teaches throttling of memory if actual current exceeds threshold (520 of Fig 5).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Trick, Abrahams, Nerl and Wu. One ordinary skill in the art would be motivated to throttle the memory, since that ensures the cooling of memory device.

6. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Trick (US Patent 5995405), in view of Abrahams et al (US Patent Application Publication 2004/0078454), further in view of Wu (US Patent 7064994).

Neither Trick nor Abrahams et al teach the throttling of the memory. Wu teaches throttling of memory if actual current exceeds threshold (Fig 5).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Trick, Abrahams and Wu. One ordinary skill in the art would be motivated to throttle the memory, since that ensures the cooling of memory device.

7. Claims 13-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abrahams et al (US Patent Application Publication 2004/0078454), in view of Nerl (US Patent Application Publication 20020016897)

For claim 13, Abrahams et al teach the following:
A method of manufacturing a memory module (101) comprising: measuring operating current values in each of a plurality of memory devices (lines 13-15 of page 1); storing each of the operating current values corresponding to each of the plurality of memory devices in a non-volatile memory device (each current is stored in a non-volatile memory of each component 100G); and forming a memory module (101) comprising each of the plurality of memory devices and the non-volatile memory device (Fig 1).

Abraham et al do not teach that the plurality of memory devices can be plurality of volatile memory devices. However, Abrahams et al teach that the plurality of memory devices can be plurality of FRU.

Neil teaches that a DIMM can be an FRU.

It would have been obvious for one ordinary skill in the art at the time the invention was made to have the DIMM as an FRU in the system of Abraham et al, since it is convenient to use DIMM as an FRU for it's hot swapping ability.

For claims 14-16, DIMMs are associated with SPD, DRAM and dual-in line memory.

For claim 17, Abrahams et al teach the following:
A method of manufacturing a memory module (101) comprising: measuring operating current values in each of a plurality of memory devices, wherein the plurality of memory corresponds to a single manufacturing lot (lines 13-15 of page 1); storing operating current values in a non-volatile memory device (current is stored in a non-volatile memory of each component 100G); and forming a memory module (101) comprising each of the plurality of memory devices and the non-volatile memory device (Fig 1).

Abraham et al do not teach that the plurality of memory devices can be plurality of volatile memory devices. However, Abrahams et al teach that the plurality of memory devices can be plurality of FRU.

Neil teaches that a DIMM can be an FRU.

It would have been obvious for one ordinary skill in the art at the time the invention was made to have the DIMM as an FRU, since it is convenient to use DIMM as an FRU for it's hot swapping ability.

Abraham et al as modified by Neil do not teach calculation of average current. One ordinary skill in the art would have been motivated to store average current corresponding to the lot in the non-volatile memory depending on his design choice.

For claims 18-20, DIMMs are associated with SPD, DRAM and dual-in line memory.

Response to Arguments

Applicant's arguments with respect to claims 1-5, 7-11, 13-32 filed on 2/21/2007 have been fully considered but they are not persuasive.

Applicant argues that cited references do not teach any device-specific or lot-specific operating current values. Instead, the cited references disclose the device-type specific information.

Examiner disagrees. The EPROM of Trick stores the information of the corresponding IMM. Therefore, the information stored in EPROM corresponds to that particular IMM. Thus, the information is device specific or lot specific. In addition, the operating currents

of Abrahams ([0009]) are component-specific (claim 1 of page 6). Therefore, these currents are lot-specific too.

Applicant's arguments on page 16-26 with respect to claims 1-5, 7-11, 13-32 are repeatation of arguments filed on 9/29/2006, which are properly addressed in action on 12/14/2006.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fahmida Rahman whose telephone number is 571-272-8159. The examiner can normally be reached on Monday through Friday 8:30 - 5:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Fahmida Rahman
Examiner
Art Unit 2116

***

THUAN N. DU
PRIMARY EXAMINER